I3C - the better I2C? (Lightning version)

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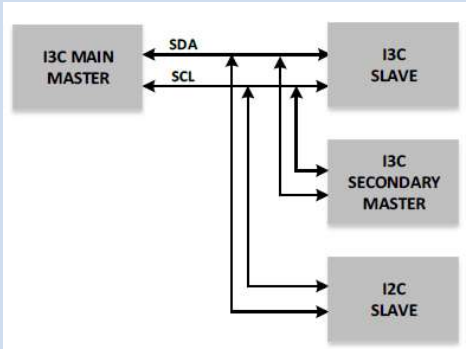
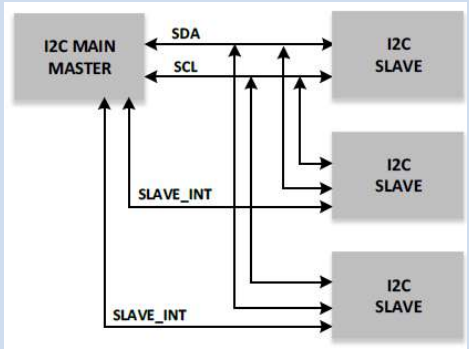
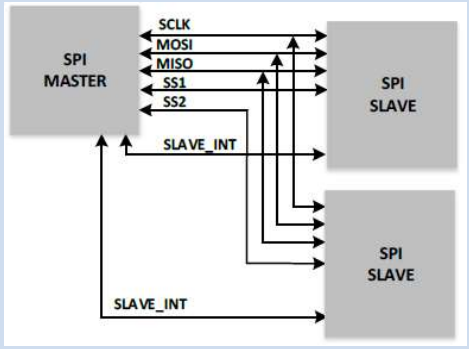
Promises

From MIPI I3C white paper 1/3

Parameter	MIPI I3C	I2C	SPI
Overview			
# of lines	2-wire	2-wire (plus separate wires for each required interrupt signal)	4-wire (plus separate wires for eachrequired interrupt signal
Effective Data Bitrate	33.3 Mbps max at 12.5 MHz (Typ.:10.6 Mbps at 12MHz SDR)	3 Mbps max at 3.4 MHz (Hs) 0.8 Mbps max at 1 MHz (Fm+) 0.35 Mbps max at 400 KHz (Fm)	Approx. 60 Mbps max at 60 MHz for conventional implementations (Typically: 10 Mbps at 10 MHz

From MIPI I3C White paper: http://resources.mipi.org/MIPI I3C-sensor-whitepaper-from-mipi-alliance

Promises

From MIPI I3C white paper 2/3

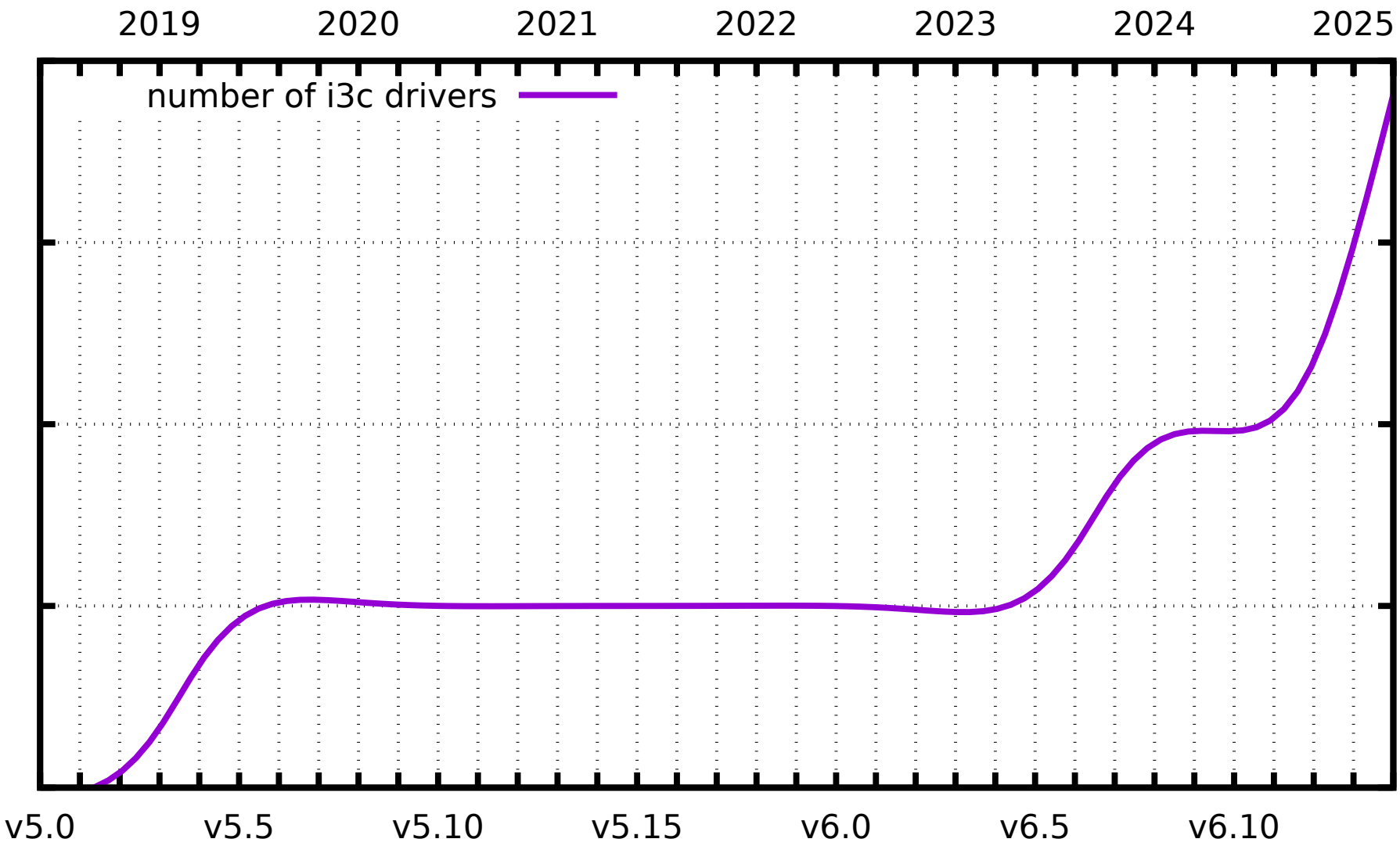
Parameter	MIPI I3C	I²C	SPI
Advantages	• Only two signal lines • Legacy I²C devices co-exist on the same bus (with some limitations) • Flexible data transmission rates • Dynamic addressing and supports static addressing for legacy I²C devices • I²C-like data rate messaging (SDR) • Optional high data rate messaging modes (HDR) • Multi-drop capability and dynamic addressing avoids collisions • Multi-master capability • In-band Interrupt support • Hot-join support • A clear master ownership and handover mechanism is defined • In-band integrated commands (CCC) Support	• Only two signal lines • Flexible data transmission rates • Each device on the bus is independently addressable • Devices have a simple master/slave relationship • Simple implementation • Widely adopted in sensor applications and beyond • Supports multi-master and multidrop capability features	• Full duplex communication • Push-pull drivers • Good signal integrity and high speed below 20MHz (higher speed are challenging) • Higher throughput than I²C and SMBus • Not limited to 8-bit words • Arbitrary choice of message size, content and purpose • Simple hardware interfacing • Lower power than I²C • No arbitration or associated failure modes • Slaves use the master's clock • Slaves do not need a unique address • Not limited by a standard to any maximum clock speed (can vary between SPI devices)

From MIPI I3C White paper: http://resources.mipi.org/MIPI I3C-sensor-whitepaper-from-mipi-alliance

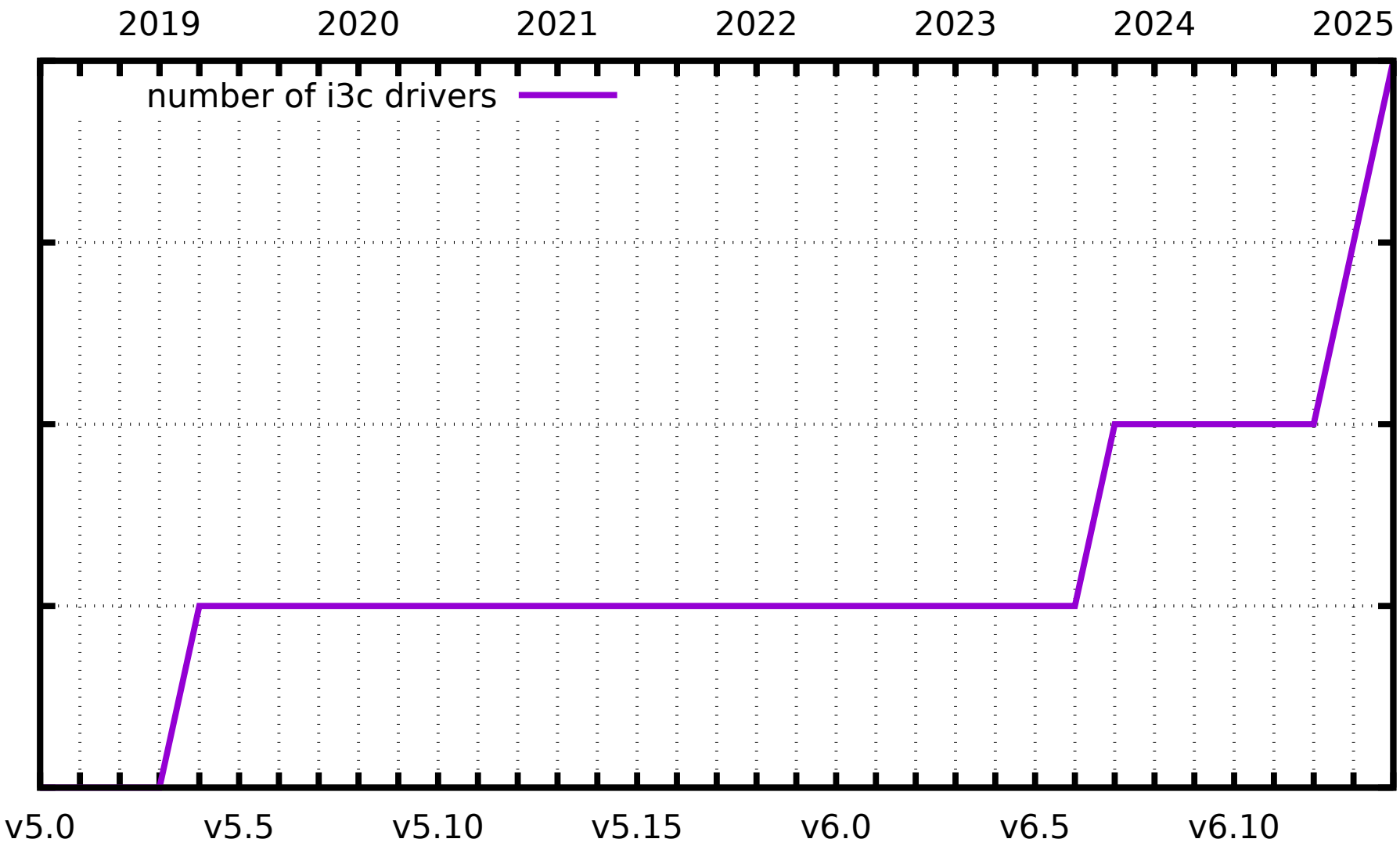
Adoption of I3C controller drivers

2018 Cadence, Designware
2020 MIPI HCI
2021 Silvaco (NXP)
2025 Qualcomm, Renesas

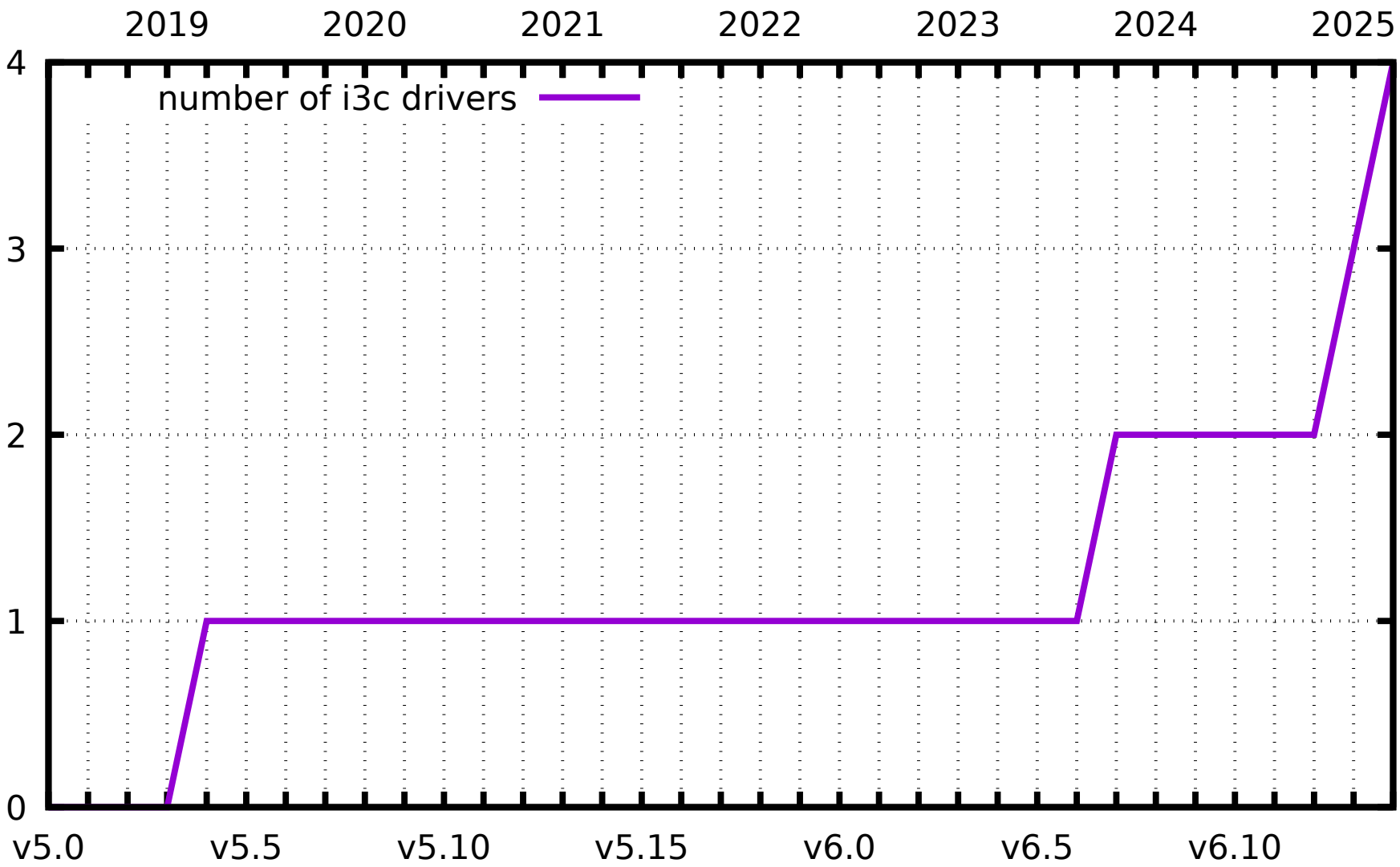
Adoption of Linux I3C target drivers



Adoption of Linux I3C target drivers



Adoption of Linux I3C target drivers



Converting an I2C driver is not hard

- Documentation is there
- I3C regmap support existed early
- what are the problems?

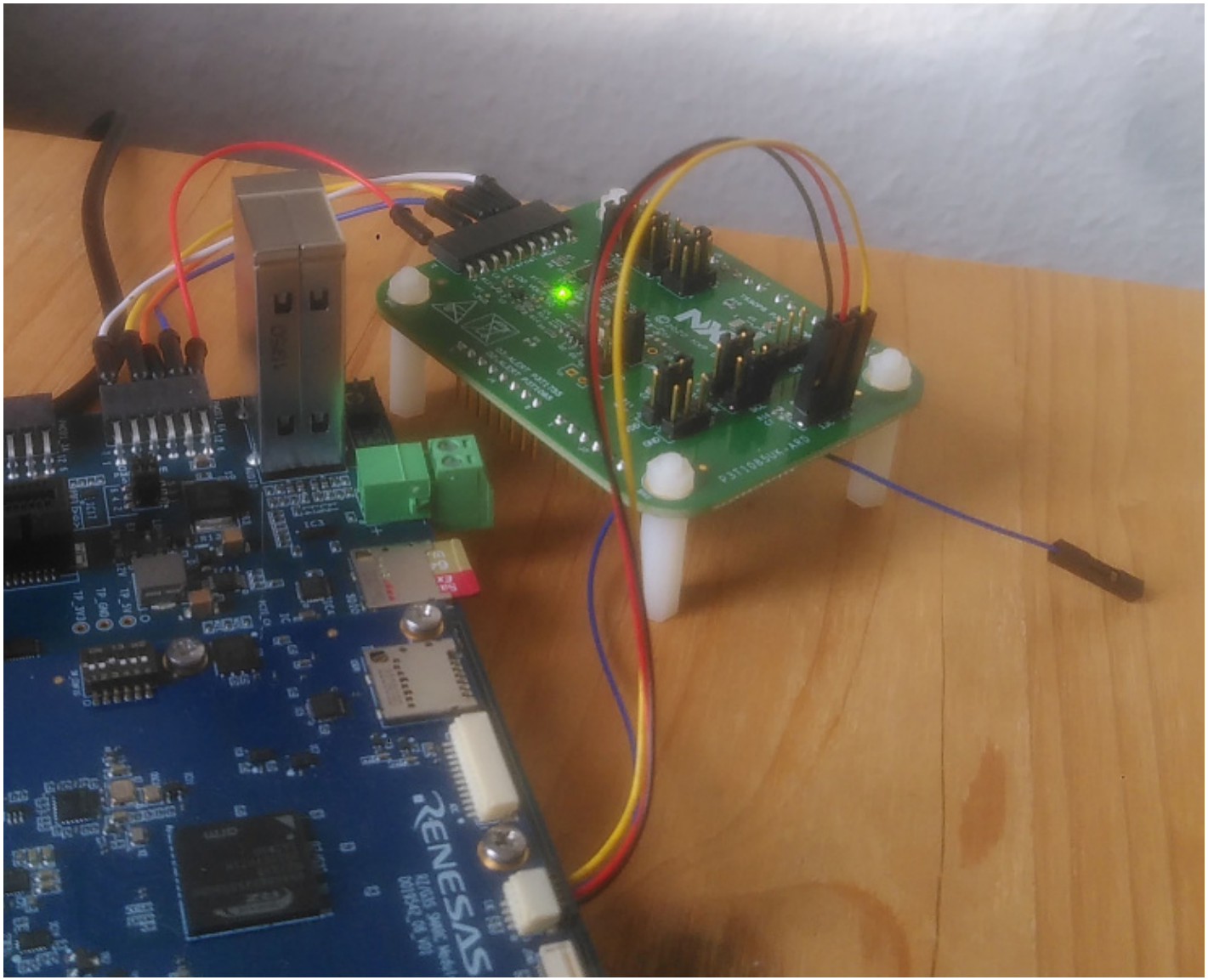
Problem: Target availability

- still only few chips available
- even fewer development boards
- for hackers too expensive

  in the $100 range
- mostly very basic I3C support

  didn't find HDR and HotJoin yet

My solution for testing a new I3C controller



Details about my solution

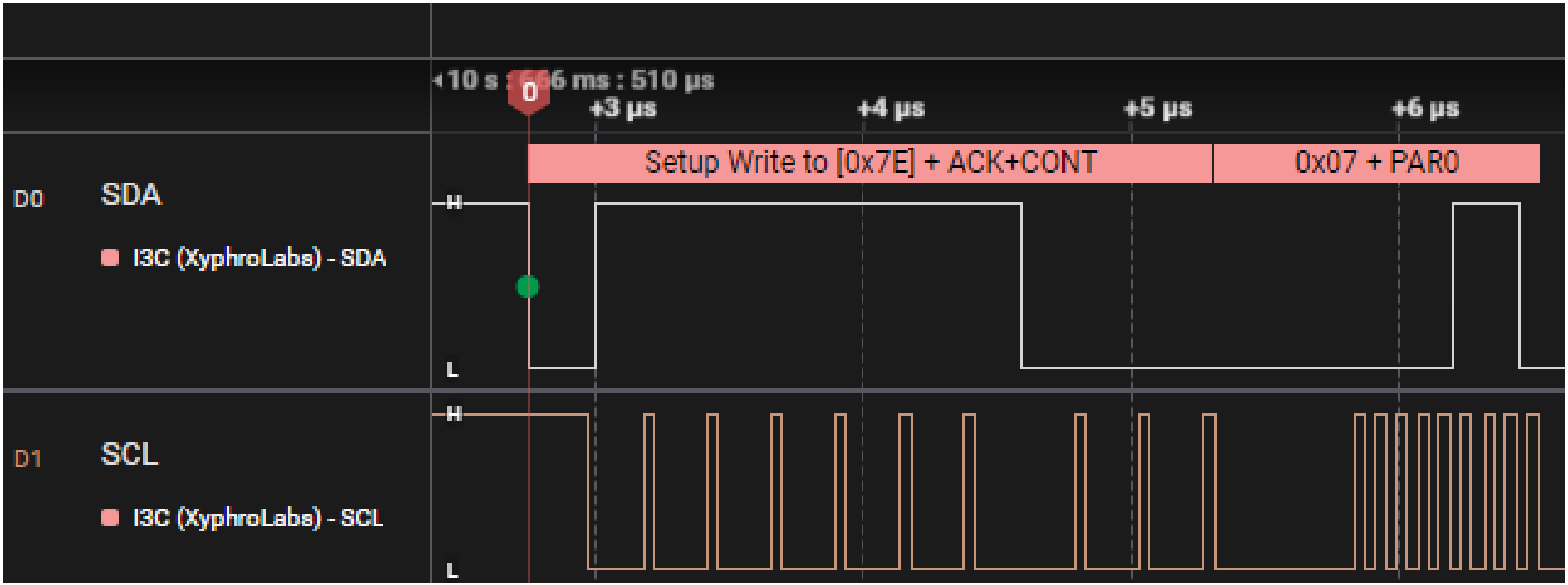
- P3T1085UK-ARD for 15€ at NXP
- added P3T1755 (free sample)
- connected I2C bus from host
- targets are supported upstream
- two I3C devices for real bus scenarios
- IBI (without payload) possible
- can handle 1.8V and 3.3V IO
- can be switched back to I2C for verification

Problem: expensive debugging tools

- USB adapters and analyzers in the €1500-€2000 range
- could not find independent reviews about them

‘Xyphro’ to the rescue

- I3C analyzer plugin for Logic2 software[1]
- source available
- worked totally fine for my cases
- true hacker’s spirit, forgot the license



[1] https://github.com/xyphro/XyphroLabs-I3C-Saleae-Protocol-Analyzer

Problem: Controller availability

Using Linux

- mostly on newer SoCs
- boards either expensive or not available yet

  in the €500 - €2000 range
- not exposed on some carrier boards by default

And outside Linux

- MCUs usually are target only
- ... or they lack software support

  Renesas EK-RA4E2 has good support for Zephyr, well, except I3C

‘Xyphro’ to the rescue again

- USB-to-I3C adapter based on Raspberry PI Pico[2]
- $<$ 10€ for board and level shifter
- MIT licensed
- supports even HDR-DDR transmissions
- haven’t tried it yet but sounds awesome

[2] https://github.com/xyphro/I3CBlaster

Problem: complexity also on the core side

Status and to-do list

- Things have moved forward
  - Hardware manufacturers more and more interested
  - Three controller drivers upstream
  - One IMU device driver upstream (not fully leveraging the power of I3C yet)
  - Ongoing controller handover work
    `https://lkml.kernel.org/lkml/1606716983-3645-1-git-send-email-pthombar@cadence.com/`
- There is still room for improvement
  - `HDR` support
  - I3C target interface
  - Global and directed resets
  - Time synchronization
  - `/dev` interface with additional user controls?
  - ...

(from late 2021)

My conclusions about I3C

- complexity shifted from hardware to software
- progress is slow, doesn't feel like it has momentum
- I3C will be used

  it made its way into specifications (DDR5, PCI Express)
- it will be mainly and slowly driven by the industry

  not very approachable for hackers
- key features will remain unsupported in Linux

  at least for a very long time
- I2C will stay around because of its simplicity
- **make I3C hackable**

This talk is heavily supported by

The End

Questions? Comments?

Questions?

- ~~Right here, right now~~ (lightning talk)
- ~~At the conference~~ (it's over after this)
- wsa@kernel.org

References

- MIPI I3C Technology by Emmanuel T. Nana / NXP, 08/2017
- I3C in tomorrow's designs by Miquel Raynal / Bootlin, Fall 2021